

## Clock OSC

## XG-2102CA

SEIKO EPSON CORPORATION

Product name XG-2102CA 100.000000MHz +/-50ppm PGSN

Product Number / Ordering code X1M0003010048xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LV-PECL

Pb free / Complies with EU RoHS directive

Reference weight Typ. 133 mg

**1.Absolute maximum ratings**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	V <sub>cc-GND</sub>	-0.5	-	4	V	-
Storage temperature	T <sub>stg</sub>	-55	-	125	°C	Storage as single product
Input voltage	V <sub>in</sub>	-0.5	-	V <sub>cc</sub> +0.5	V	ST or OE Terminal

**2.Specifications(characteristics)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f <sub>0</sub>	-	100.0000	-	MHz	
Supply voltage	V <sub>cc</sub>	2.97	3.3	3.63	V	-
Operating temperature	T <sub>use</sub>	-20	-	70	°C	-
Frequency tolerance	f <sub>tol</sub>	-50	-	50	x10 <sup>-6</sup>	-
Current consumption	I <sub>cc</sub>	-	-	60	mA	OE=V <sub>cc</sub> , L_ECL=50ohm
Stand-by current	I <sub>std</sub>	-	-	-	mA	-
Disable current	I <sub>dis</sub>	-	-	2.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	As output crodding point
Output voltage(LV-PECL)	V <sub>OH</sub>	V <sub>cc</sub> -1.025	2.35	V <sub>cc</sub> -0.88	V	-
	V <sub>OL</sub>	V <sub>cc</sub> -1.81	1.6	V <sub>cc</sub> -1.62	V	-
Output load condition(ECL)	L <sub>ECL</sub>	-	50	-	Ω	Terminated to V <sub>cc</sub> -2.0V
Input voltage	V <sub>IH</sub>	70% V <sub>cc</sub>	-	-		OE Terminal
	V <sub>IL</sub>	-	-	30% V <sub>cc</sub>		OE Terminal
Rise time	t <sub>r</sub>	-	-	400	ps	At 20% to 80% output swing
Fall time	t <sub>f</sub>	-	-	400	ps	At 20% to 80% output swing
Start-up time	t <sub>str</sub>	-	-	10	ms	-
Jitter	t <sub>DJ</sub>	-	-	N/A	ps	Deterministic Jitter
	T <sub>RJ</sub>	-	-	N/A	ps	Random Jitter
	t <sub>RMS</sub>	-	-	N/A	ps	δ(RMS of total distribution)
	t <sub>p-p</sub>	-	-	N/A	ps	Peak to Peak
	t <sub>acc</sub>	-	-	N/A	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t <sub>PJ</sub>	-	-	0.23	ps	Off set Frequency: 12kHz to 20MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Off set 1Hz
		-	-62.0	-	dBc/Hz	Off set 10Hz
		-	-91.9	-	dBc/Hz	Off set 100Hz
		-	-121.1	-	dBc/Hz	Off set 1kHz
		-	-144.8	-	dBc/Hz	Off set 10kHz
		-	-152.9	-	dBc/Hz	Off set 100kHz
		-	-155.4	-	dBc/Hz	Off set 1MHz
Frequency aging	f <sub>age</sub>	-10	-	10	x10 <sup>-6</sup> /Year	@ +25°C first year

### 3. Test circuit

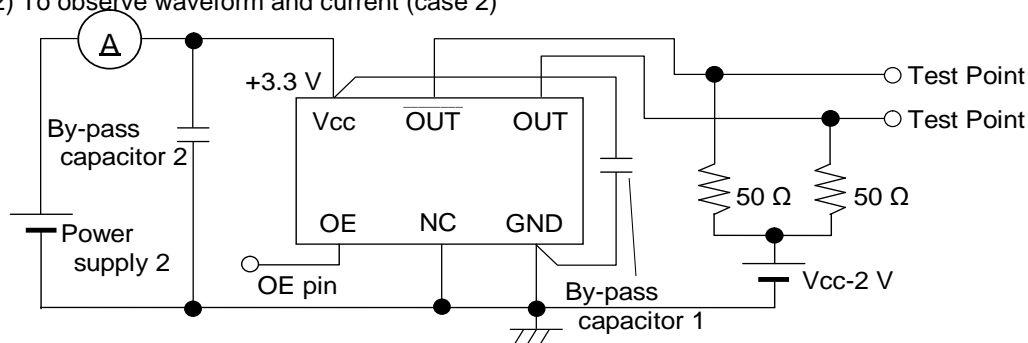
1) To observe waveform and current (case 1)



\* The lines from OUT and  $\overline{\text{OUT}}$  pin are same length.

\* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



\* The lines from OUT and  $\overline{\text{OUT}}$  pin are same length.

\* To measure the disable current, OE pin is connected to GND

3) Measurement condition

A) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) places closely between Vcc and GND.

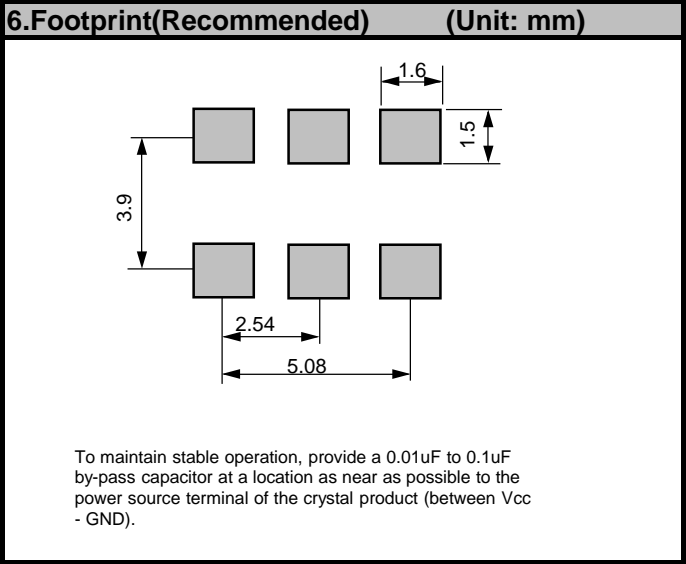
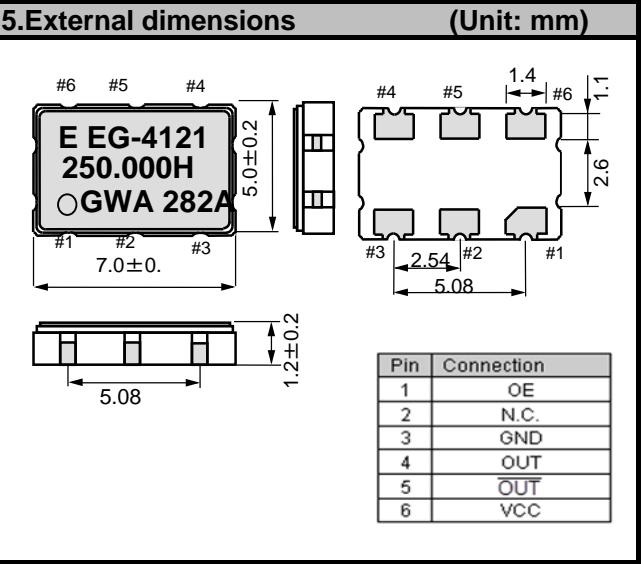
C) By-pass capacitor 2 (approx. 10  $\mu\text{F}$ ) places closely between power supply terminals on the board.

D) Use the current meter whose internal impedance value is small.

E) Power supply

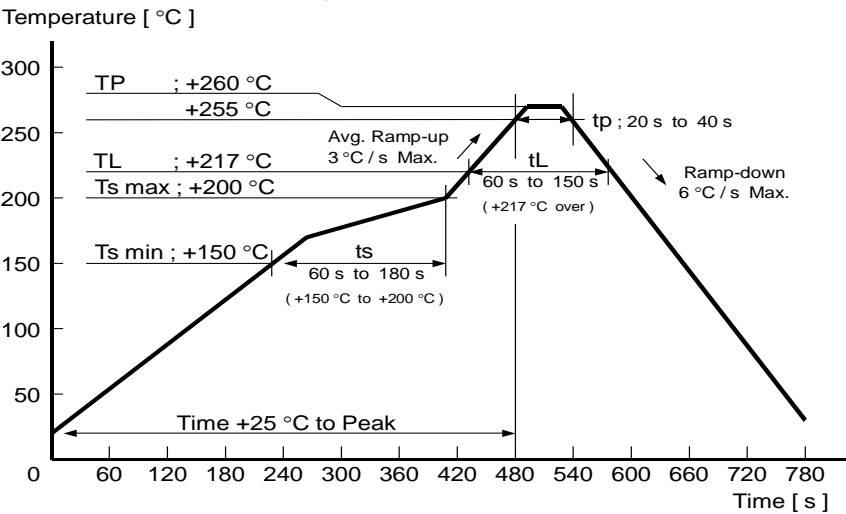
- Start up time (0 Vg90 %Vcc) of power source should be more than 150  $\mu\text{s}$  and slew rate should be less than 19.8 mV/ $\mu\text{s}$ .
- Impedance of power supply should be as low as possible.

4.Timing chart



7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



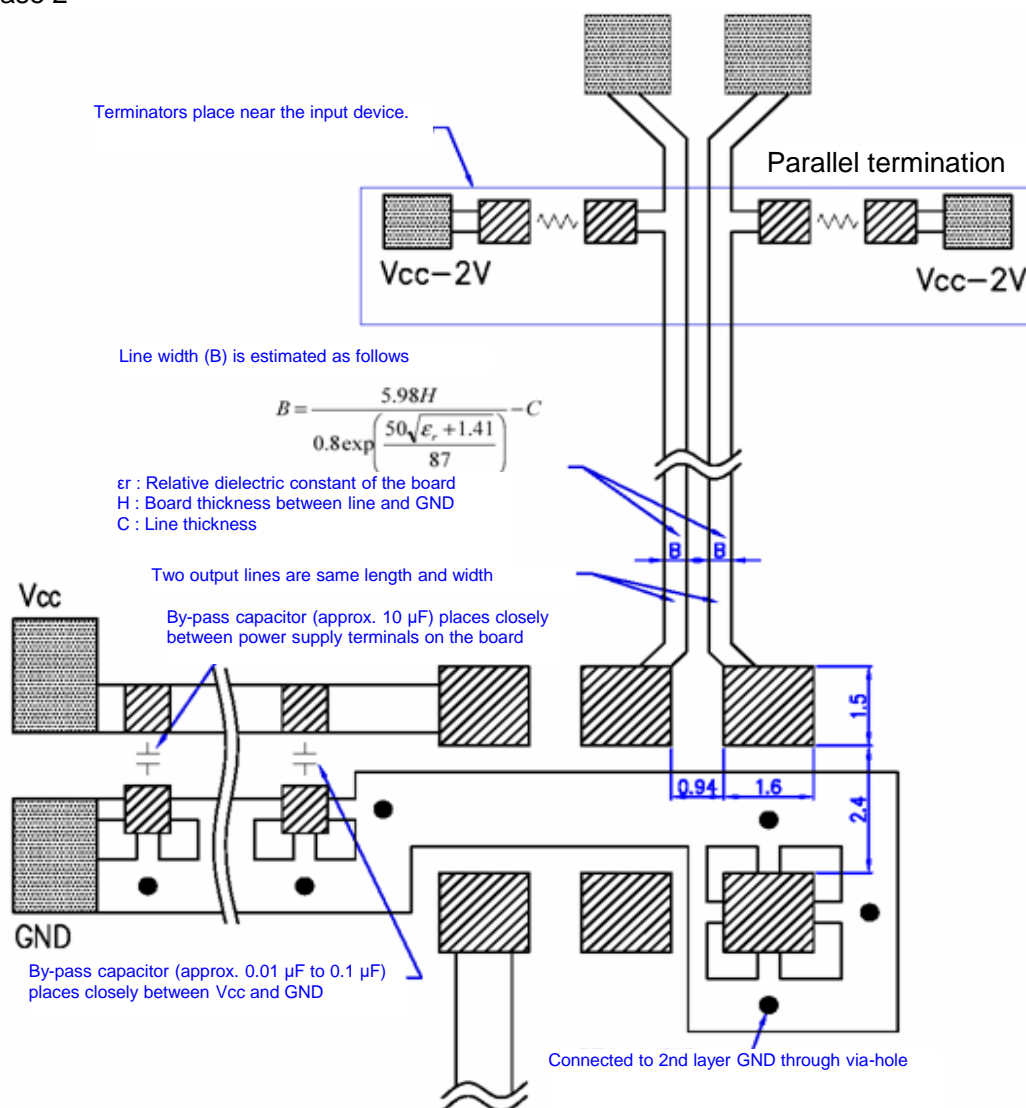
## 8.PCB layout (2 layers, 2nd layer is all GND pattern)

## Case 1



- \* By-pass capacitor (approx. 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) places closely between Vcc and GND.
- \* By-pass capacitor (approx. 10  $\mu\text{F}$ ) places closely between power supply terminals on the board.
- \* Please design the two output lines by characteristic impedance 50  $\Omega$  and same length, and try to make the output lines as short as possible.
- \* Terminators place near the input device.

## Case 2



- \* By-pass capacitor (approx. 0.01  $\mu$ F to 0.1  $\mu$ F) places closely between Vcc and GND.
- \* By-pass capacitor (approx. 10  $\mu$ F) places closely between power supply terminals on the board.
- \* Please design the two output lines by characteristic impedance 50  $\Omega$  and same length, and try to make the output lines as short as possible.
- \* Terminators place near the input device.

## 9.Packing information

[ 1 ] Product number last 2 digits code(xx) description

The recommended code is "00"

X1M0003010048xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

## [ 2 ] Taping specification

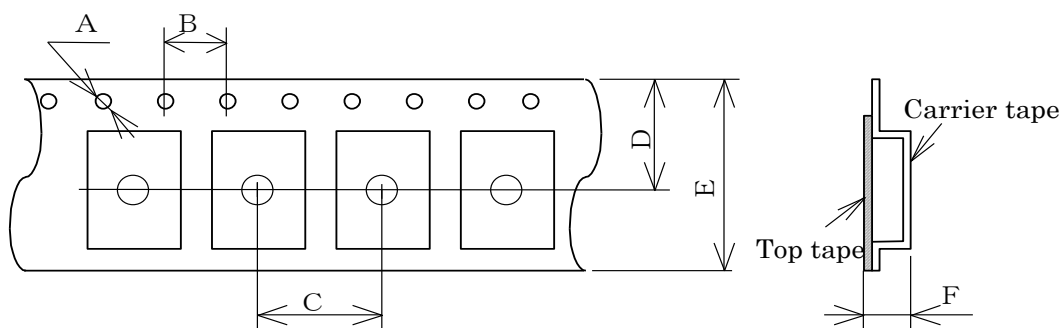
Subject to EIA-481 &amp; IEC-60286

## (1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

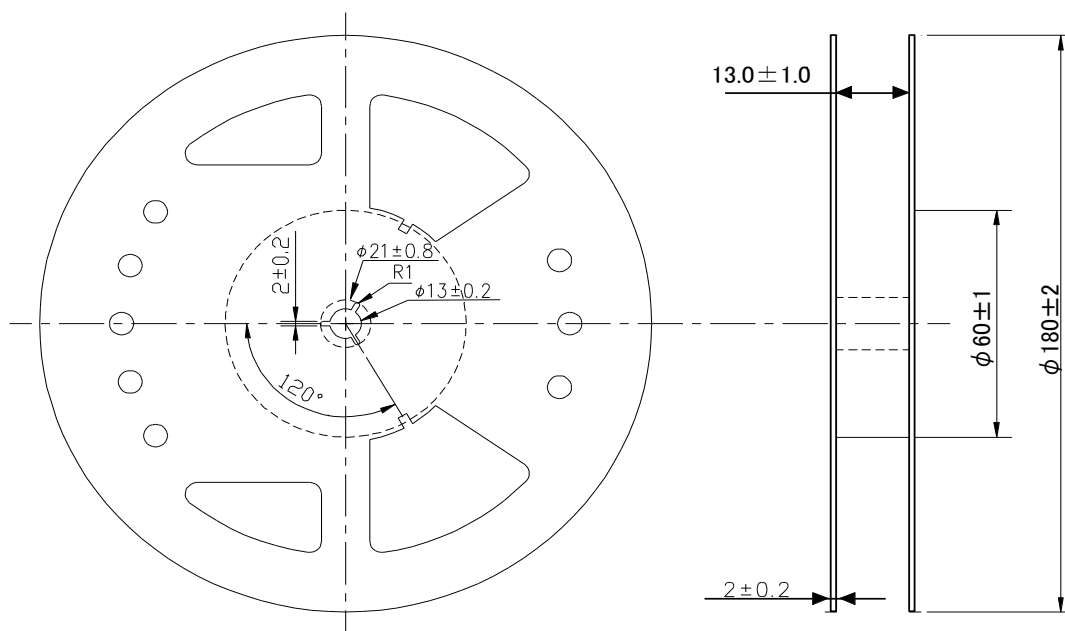


Symbol	A	B	C	D	E	F
Value	$\phi 1.5$	4	8	9.25	16	2.3

## (2) Reel dimensions

Center material : PS

Material of the Reel : PS



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