

Clock OSC

XG-2121CA

SEIKO EPSON CORPORATION

Product name XG-2121CA 125.000000MHz +/-50ppm PGPA

Product Number / Ordering code X1M0003110014xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LV-PECL

Pb free / Complies with EU RoHS directive

Reference weight Typ. 133 mg

1.Absolute maximum ratings

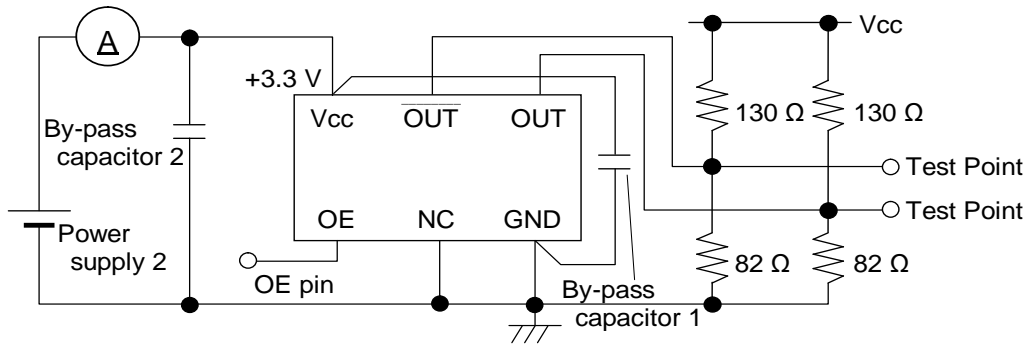
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	V _{cc-GND}	-0.5	-	4	V	-
Storage temperature	T _{stg}	-55	-	125	°C	Storage as single product
Input voltage	V _{in}	-0.5	-	V _{cc} +0.5	V	ST or OE Terminal

2.Specifications(characteristics)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f ₀	-	125.0000	-	MHz	
Supply voltage	V _{cc}	2.375	2.5	2.625	V	-
Operating temperature	T _{use}	0	-	70	°C	-
Frequency tolerance	f _{tol}	-50	-	50	x10 ⁻⁶	-
Current consumption	I _{cc}	-	-	60	mA	OE=V _{cc} , L_ECL=50ohm
Stand-by current	I _{std}	-	-	-	mA	-
Disable current	I _{dis}	-	-	2.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	As output crodding point
Output voltage(LV-PECL)	V _{OH}	V _{cc} -1.025	1.55	V _{cc} -0.88	V	-
	V _{OL}	V _{cc} -1.81	0.8	V _{cc} -1.62	V	-
Output load condition(ECL)	L _{ECL}	-	50	-	Ω	Terminated to V _{cc} -2.0V
Input voltage	V _{IH}	30% V _{cc}	-	-		OE Terminal
	V _{IL}	-	-	30% V _{cc}		OE Terminal
Rise time	t _r	-	-	400	ps	At 20% to 80% output swing
Fall time	t _f	-	-	400	ps	At 20% to 80% output swing
Start-up time	t _{str}	-	-	10	ms	-
Jitter	t _{DJ}	-	-	N/A	ps	Deterministic Jitter
	T _{RJ}	-	-	N/A	ps	Random Jitter
	t _{RMS}	-	-	N/A	ps	δ(RMS of total distribution)
	t _{p-p}	-	-	N/A	ps	Peak to Peak
	t _{acc}	-	-	N/A	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t _{PJ}	-	-	0.23	ps	Off set Frequency: 12kHz to 20MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Off set 1Hz
		-	-54.9	-	dBc/Hz	Off set 10Hz
		-	-87.0	-	dBc/Hz	Off set 100Hz
		-	-116.2	-	dBc/Hz	Off set 1kHz
		-	-145.3	-	dBc/Hz	Off set 10kHz
		-	-151.9	-	dBc/Hz	Off set 100kHz
		-	-153.7	-	dBc/Hz	Off set 1MHz
Frequency aging	f _{age}	-	-	-	x10 ⁻⁶ /Year	Included in Frequency tolerance 10 years

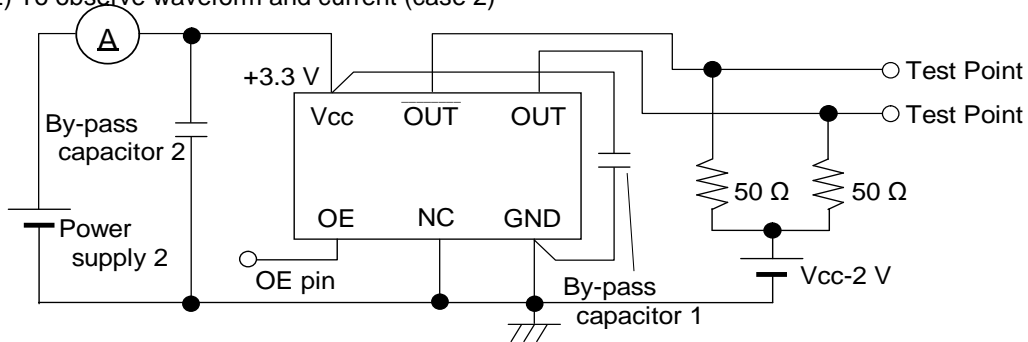
3. Test circuit

1) To observe waveform and current (case 1)



- * The lines from OUT and $\overline{\text{OUT}}$ pin are same length.
- * To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



- * The lines from OUT and $\overline{\text{OUT}}$ pin are same length.
- * To measure the disable current, OE pin is connected to GND

3) Measurement condition

A) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01 μF to 0.1 μF) places closely between Vcc and GND.

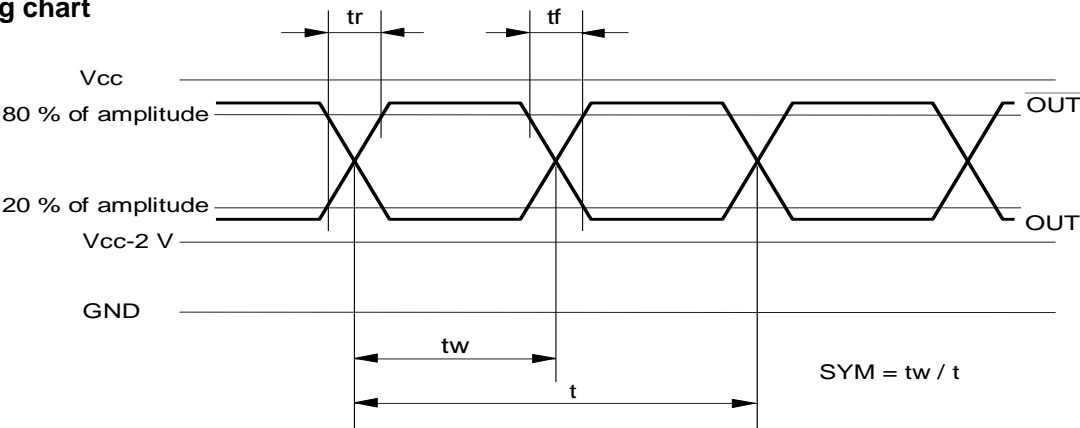
C) By-pass capacitor 2 (approx. 10 μF) places closely between power supply terminals on the board.

D) Use the current meter whose internal impedance value is small.

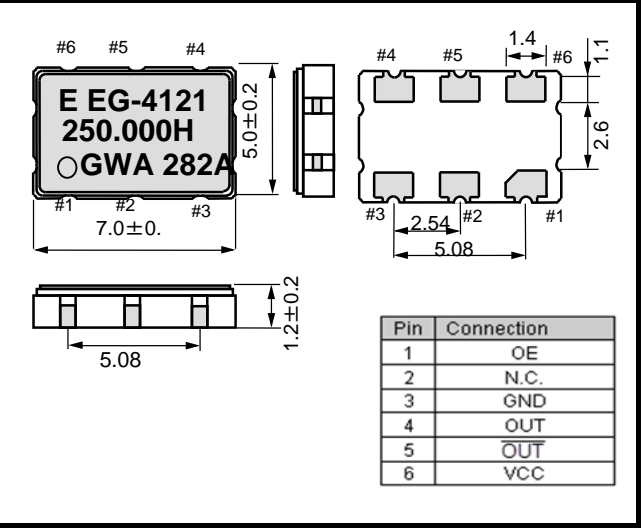
E) Power supply

- Start up time (0 Vg90 %Vcc) of power source should be more than 150 μs and slew rate should be less than 19.8 mV/ μs .
- Impedance of power supply should be as low as possible.

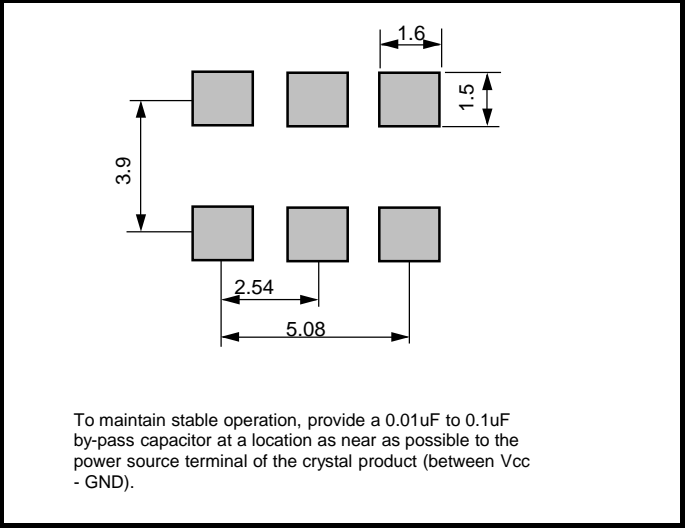
4.Timing chart



5.External dimensions (Unit: mm)



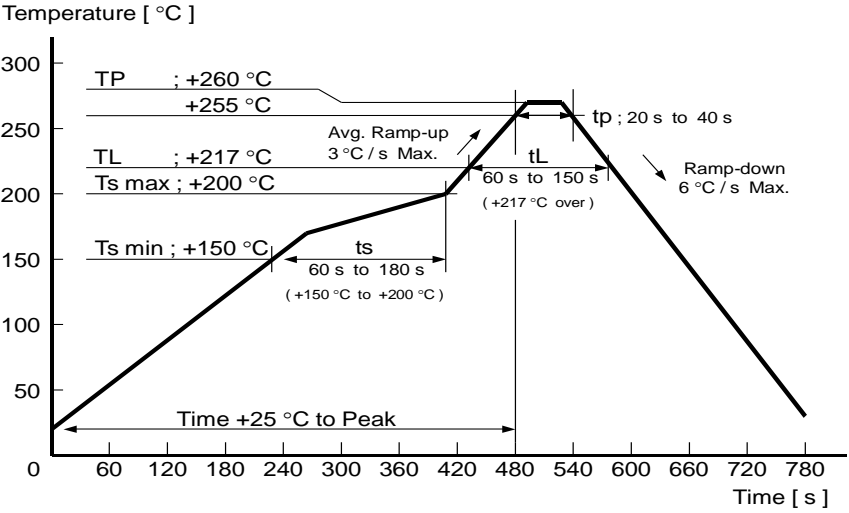
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

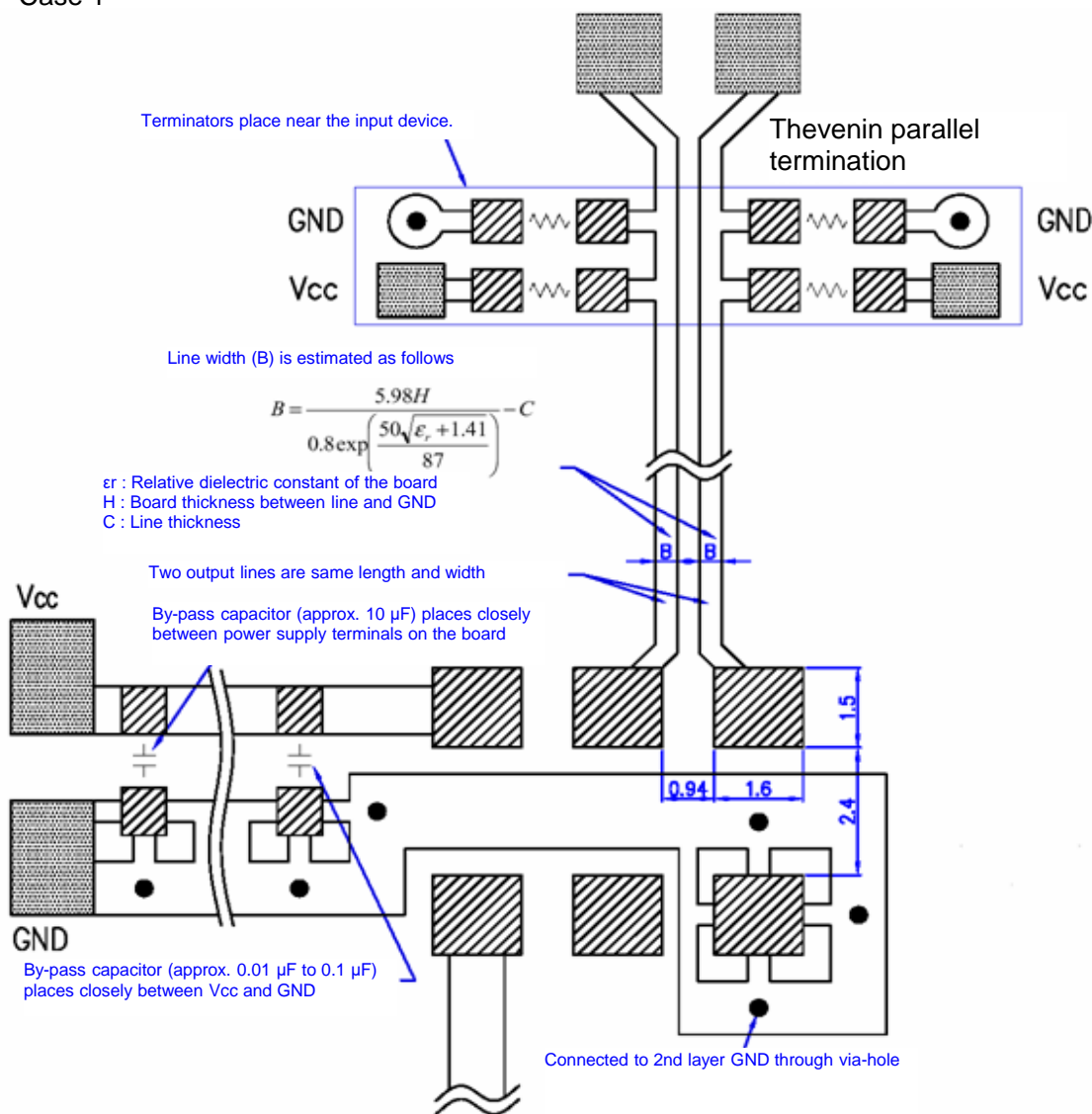
7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



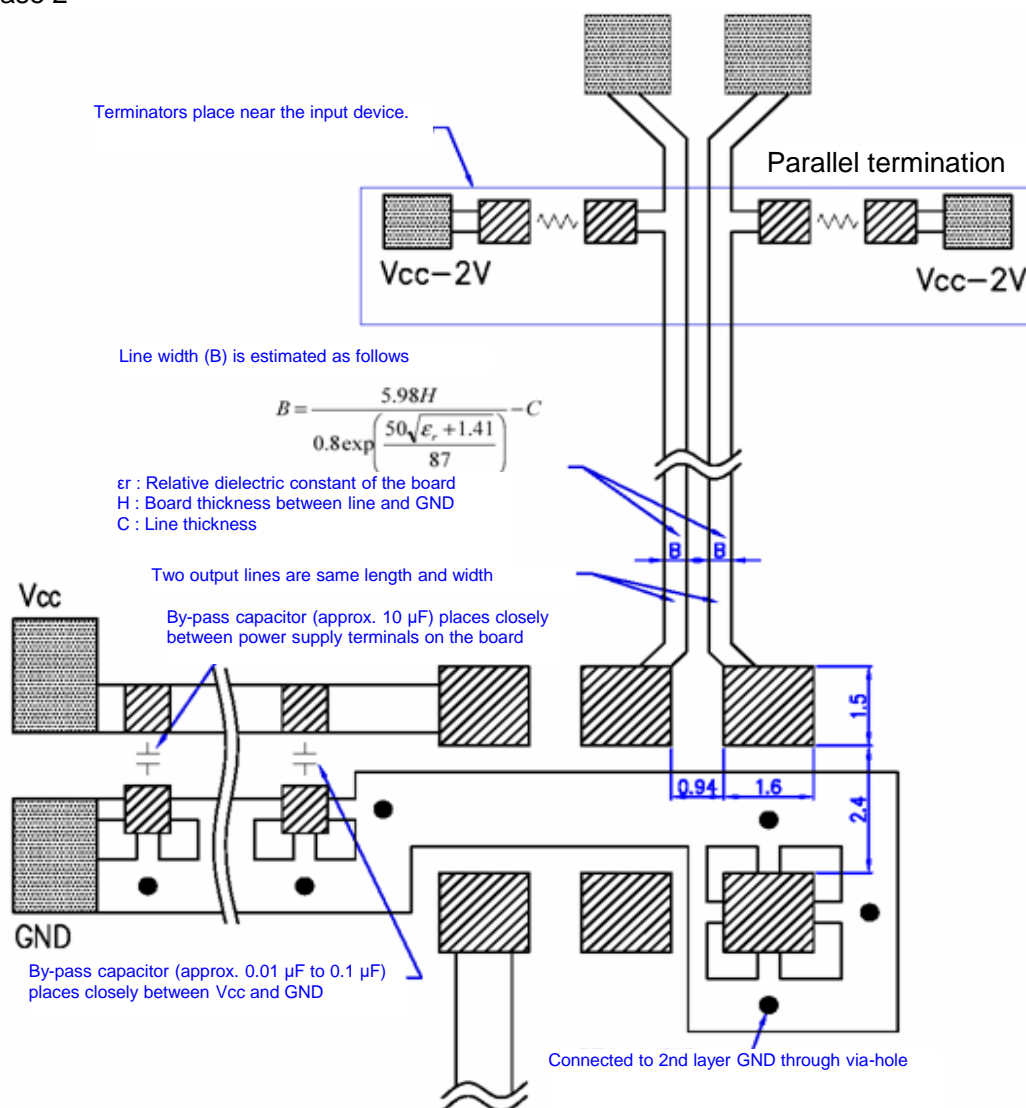
8.PCB layout (2 layers, 2nd layer is all GND pattern)

Case 1



- * By-pass capacitor (approx. 0.01 μ F to 0.1 μ F) places closely between Vcc and GND.
- * By-pass capacitor (approx. 10 μ F) places closely between power supply terminals on the board.
- * Please design the two output lines by characteristic impedance 50 Ω and same length, and try to make the output lines as short as possible.
- * Terminators place near the input device.

Case 2



- * By-pass capacitor (approx. 0.01 μ F to 0.1 μ F) places closely between Vcc and GND.
- * By-pass capacitor (approx. 10 μ F) places closely between power supply terminals on the board.
- * Please design the two output lines by characteristic impedance 50 Ω and same length, and try to make the output lines as short as possible.
- * Terminators place near the input device.

9.Packing information

[1] Product number last 2 digits code(xx) description

The recommended code is "00"

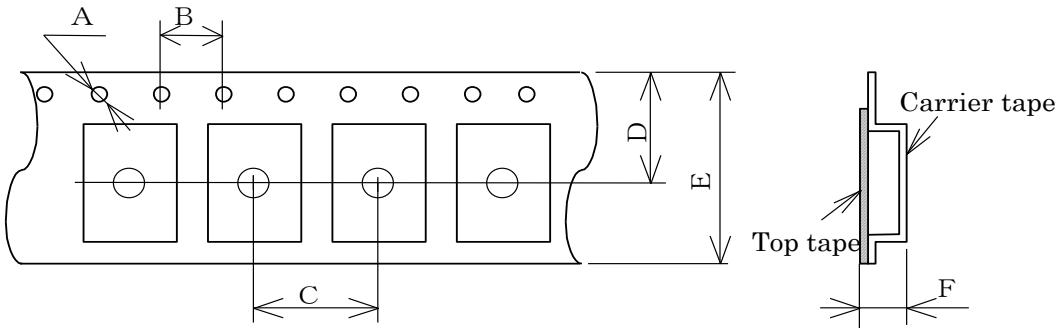
X1M0003110014xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[2] Taping specification
Subject to EIA-481 & IEC-60286

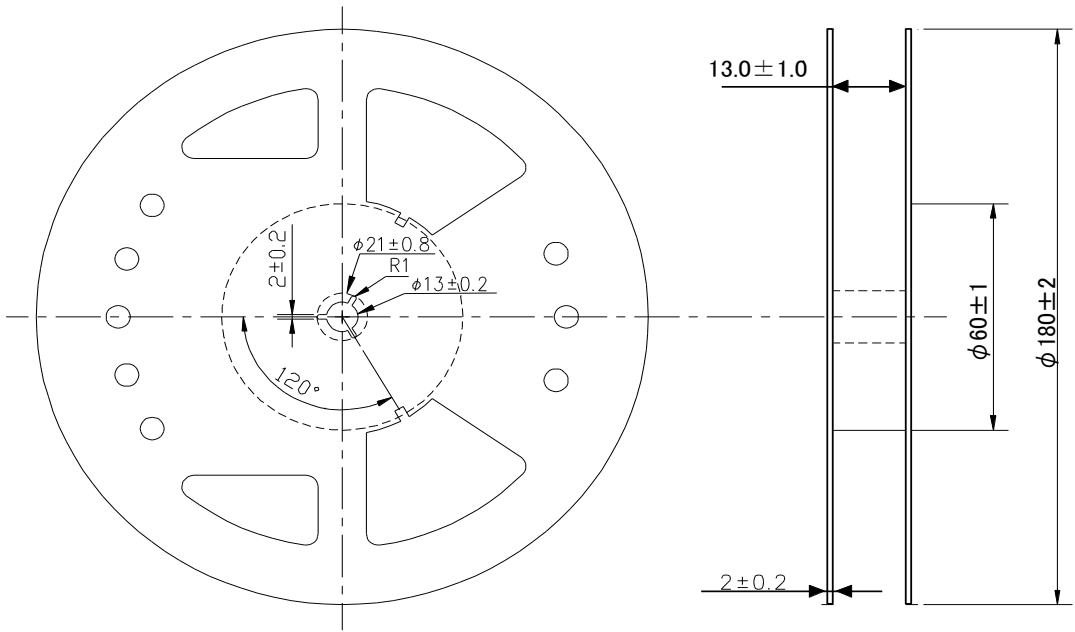
- (1) Tape dimensions
Material of the Carrier Tape : PS
Material of the Top Tape : PET+PE

Unit: mm



Symbol	A	B	C	D	E	F
Value	$\phi 1.5$	4	8	9.25	16	2.3

- (2) Reel dimensions
Center material : PS
Material of the Reel : PS



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