

Clock OSC

XG-2121CA

SEIKO EPSON CORPORATION

Product name XG-2121CA 133.330000MHz +/-50ppm LGRN

Product Number / Ordering code X1M0003510002xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LVDS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 133 mg

**1.Absolute maximum ratings**

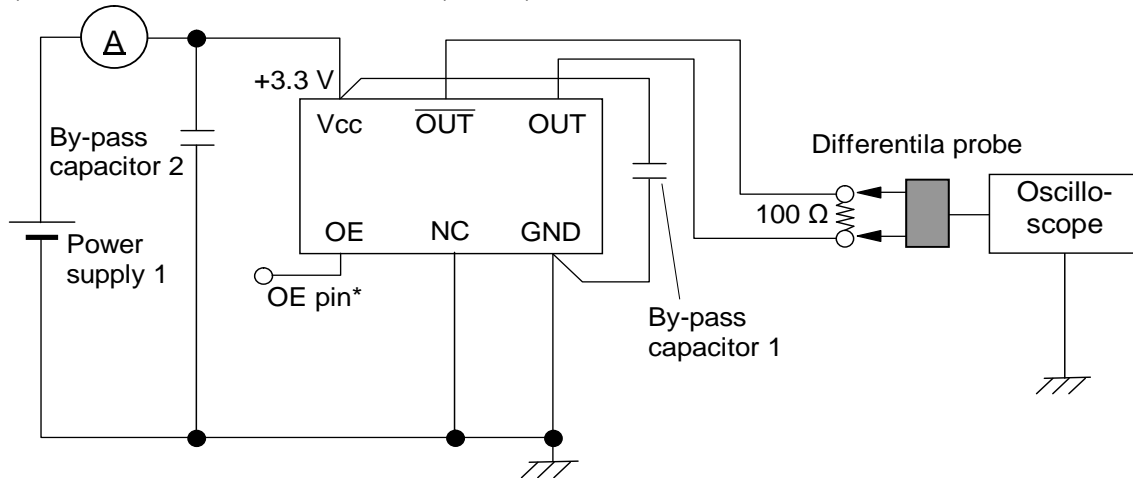
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	V <sub>cc</sub> -GND	-0.5	-	4	V	-
Storage temperature	T <sub>stg</sub>	-55	-	125	°C	Storage as single product
Input voltage	V <sub>in</sub>	-0.5	-	V <sub>cc</sub> +0.5	V	OE Terminal

**2.Specifications(characteristics)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f <sub>0</sub>	-	133.3300	-	MHz	-
Supply voltage	V <sub>cc</sub>	-0.5	-	4	V	-
Operating temperature	T <sub>use</sub>	-5	-	85	°C	-
Frequency tolerance	f <sub>tol</sub>	-50	-	50	x10 <sup>-6</sup>	-
Current consumption	I <sub>cc</sub>	-	-	30	mA	-
Stand-by current	I <sub>std</sub>	-	-	-	mA	-
Disable current	I <sub>dis</sub>	-	-	15.0	mA	-
Symmetry	SYM	45	-	55	%	-
Output voltage(LVDS)	V <sub>OD</sub>	247	-	454	mV	-
	dV <sub>OD</sub>	-	-	50	mV	-
	V <sub>os</sub>	1.125	-	1.375	V	-
	dV <sub>os</sub>	-	-	150	mV	-
Output load condition(LVDS)	L <sub>LVDS</sub>	-	100	-	Ω	-
Input voltage	V <sub>IH</sub>	0.7V <sub>cc</sub>	-	-		-
	V <sub>IL</sub>	-	-	0.3V <sub>cc</sub>		-
Rise time	t <sub>r</sub>	-	-	400	ps	-
Fall time	t <sub>f</sub>	-	-	400	ps	-
Start-up time	t <sub>str</sub>	-	-	10	ms	-
Jitter	t <sub>DJ</sub>	-	-	N/A	ps	Deterministic Jitter
	T <sub>RJ</sub>	-	-	N/A	ps	Random Jitter
	t <sub>RMS</sub>	-	-	N/A	ps	δ(RMS of total distribution)
	t <sub>p-p</sub>	-	-	N/A	ps	Peak to Peak
	t <sub>acc</sub>	-	-	N/A	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t <sub>PJ</sub>	-	-	0.27	ps	Off set Frequency: 12kHz to 20MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Off set 1Hz
		-	-49.1	-	dBc/Hz	Off set 10Hz
		-	-77.3	-	dBc/Hz	Off set 100Hz
		-	-106.7	-	dBc/Hz	Off set 1kHz
		-	-136.6	-	dBc/Hz	Off set 10kHz
		-	-147.3	-	dBc/Hz	Off set 100kHz
		-	-150.9	-	dBc/Hz	Off set 1MHz
Frequency aging	f <sub>age</sub>	-10	-	10	x10 <sup>-6</sup> /Year	@+25°C first year
		-	-	-		-

### 3. Test circuit

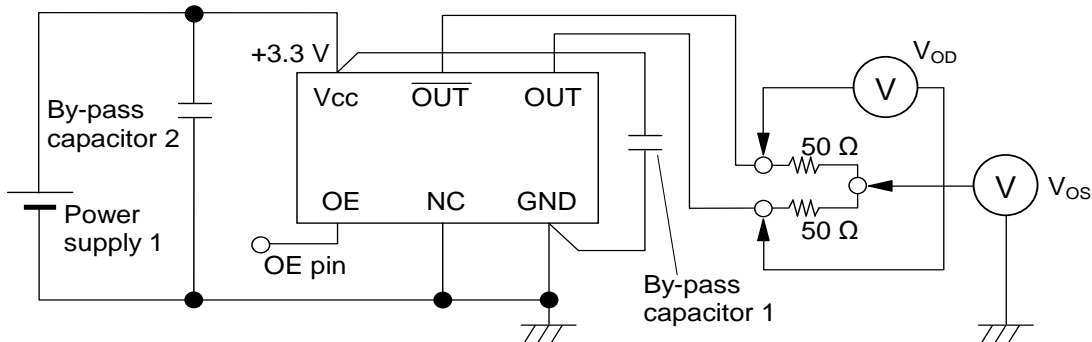
1) To observe waveform and current (case 1)



\* The lines from OUT and OUT pin are same length.

\* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



\* The lines from OUT and OUT pin are same length.

3) Measurement condition

A) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01  $\mu$ F to 0.1  $\mu$ F) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10  $\mu$ F) places closely between power supply terminals on the board.

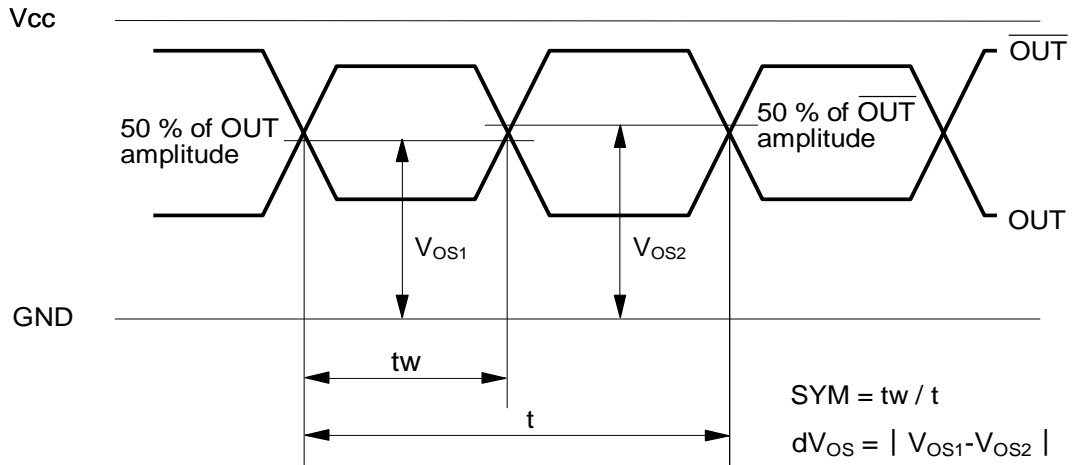
D) Use the current meter whose internal impedance value is small.

E) Power supply

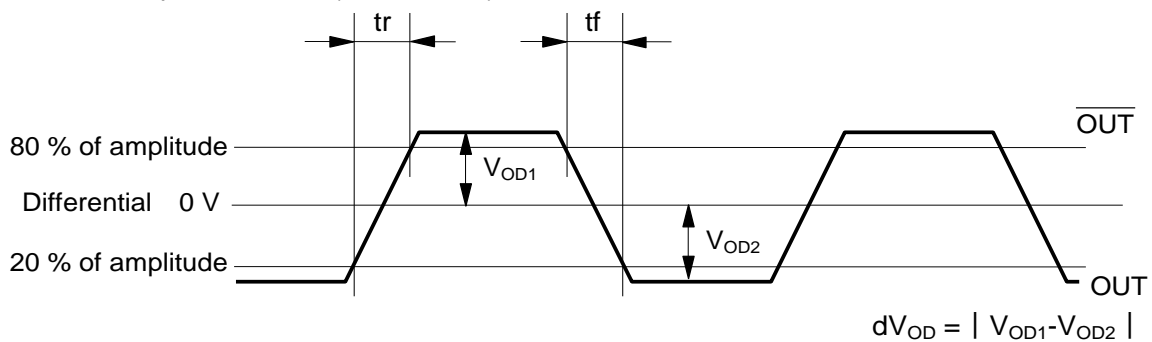
- Start up time (0 Vg90 %Vcc) of power source should be more than 150  $\mu$ s and slew rate should be less than 19.8 mV/ $\mu$ s.
- Impedance of power supply should be as low as possible.

#### 4. Timing chart

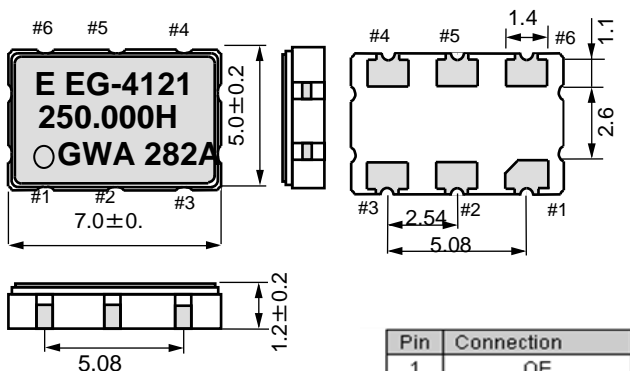
Each output waveform (OUT, and  $\overline{\text{OUT}}$ )



Differential output waveform (OUT –  $\overline{\text{OUT}}$ )

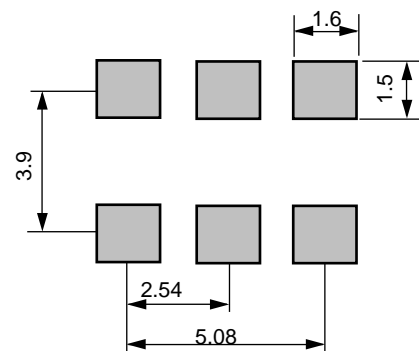


#### 5. External dimensions (Unit: mm)



Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{\text{OUT}}$
6	VCC

#### 6. Footprint (Recommended) (Unit: mm)

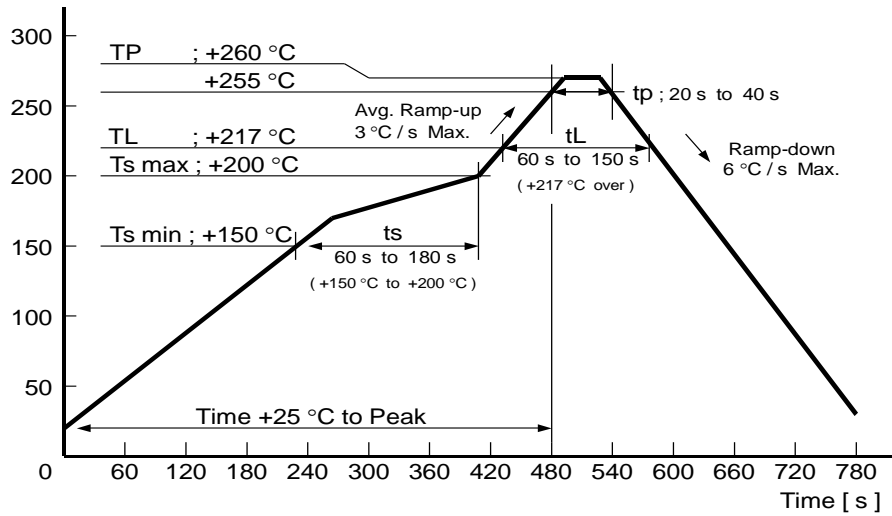


To maintain stable operation, provide a 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$  by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

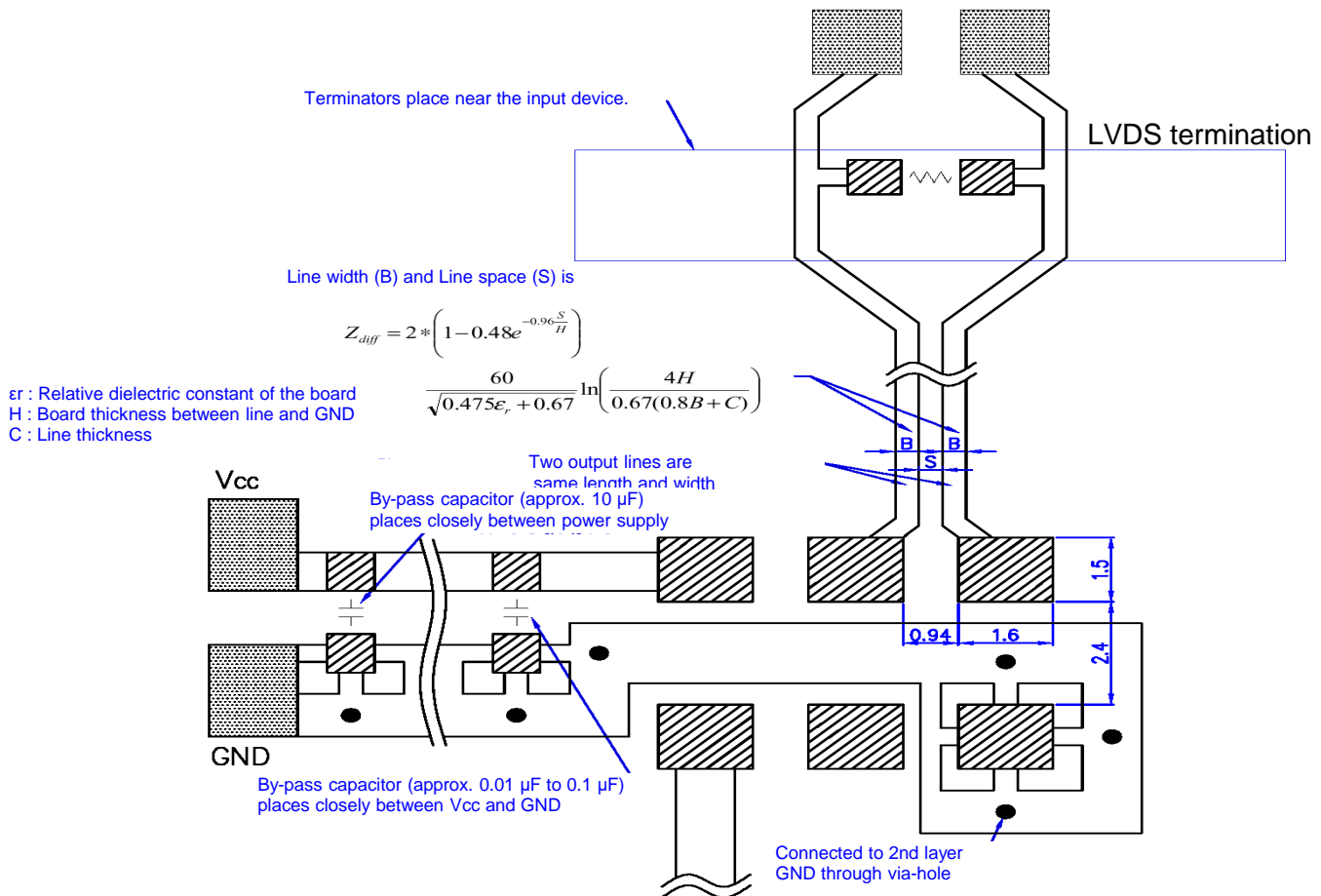
## 7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)

Temperature [ °C ]



## 8.PCB layout (2 layers, 2nd layer is all GND pattern)



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- \* By-pass capacitor (approx. 0.01  $\mu$ F to 0.1  $\mu$ F) places closely between Vcc and GND.
- \* By-pass capacitor (approx. 10  $\mu$ F) places closely between power supply terminals on the board.
- \* Please design the two output lines by characteristic impedance 100  $\Omega$  and same length, and try to make the output lines as short as possible.

### 9.Packing information

[ 1 ]Product number last 2 digits code(xx) description

The recommended code is "00"

X1M0003510002xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

## [ 2 ] Taping specification

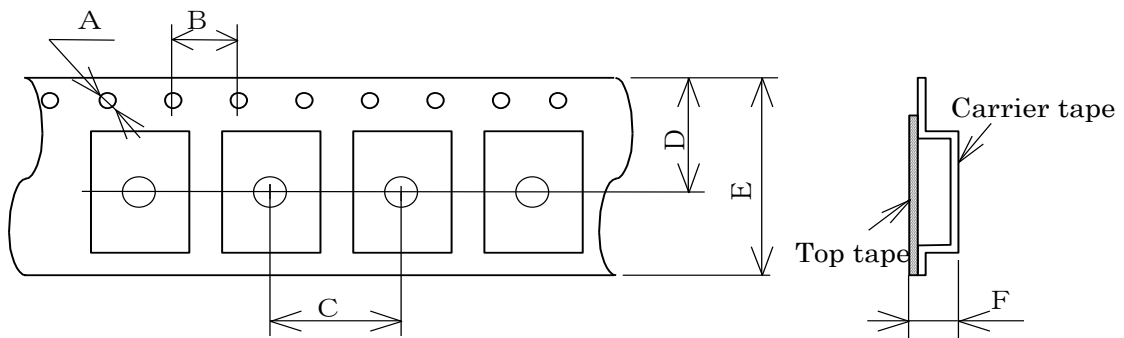
Subject to EIA-481 &amp; IEC-60286

## (1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

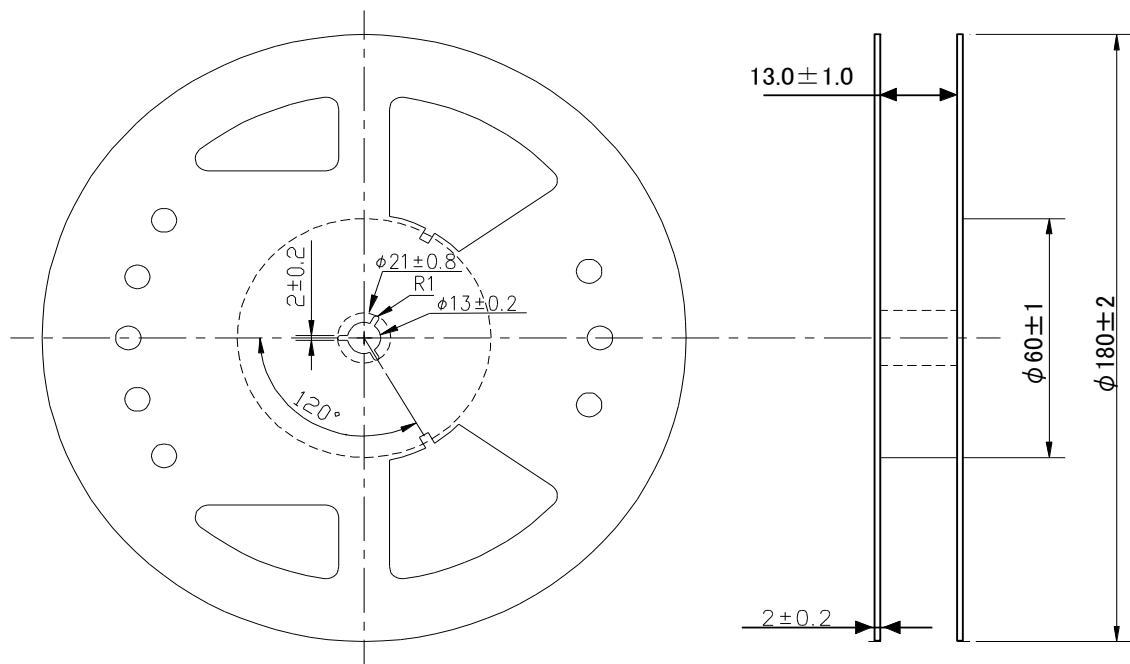


Symbol	A	B	C	D	E	F
Value	$\phi 1.5$	4	8	9.25	16	2.3

## (2) Reel dimensions

Center material : PS

Material of the Reel : PS



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