

Product name XG-2121CA 322.265625MHz +/-50ppm LGRN

Product Number / Ordering code X1M0003510030xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LVDS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 133 mg

1.Absolute maximum ratings

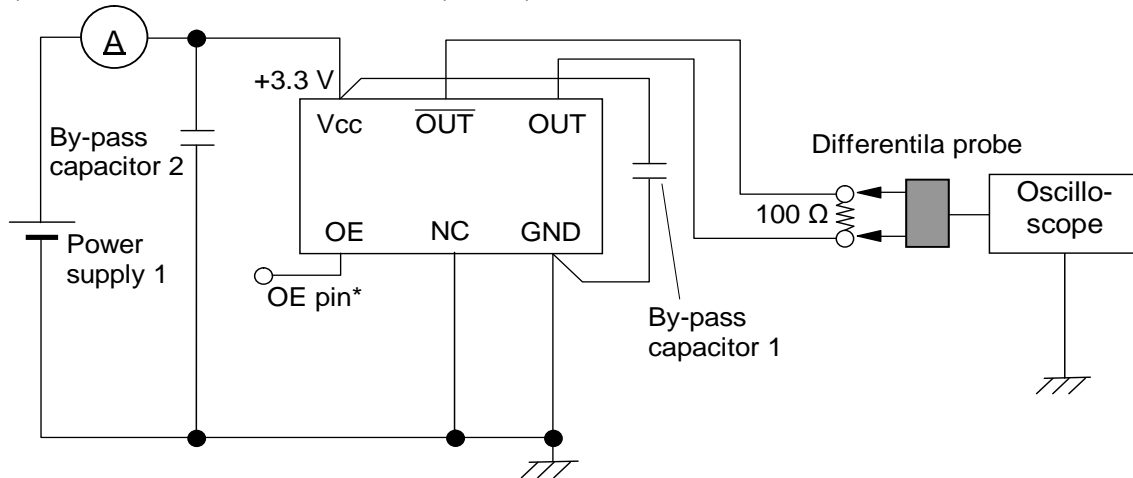
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions / Remarks |
|------------------------|---------|------|------|---------|------|---------------------------|
| Maximum supply voltage | Vcc-GND | -0.5 | - | 4 | V | - |
| Storage temperature | T_stg | -55 | - | 125 | °C | Storage as single product |
| Input voltage | Vin | -0.5 | - | Vcc+0.5 | V | OE Terminal |

2.Specifications(characteristics)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions / Remarks |
|-----------------------------|------------------|--------|----------|--------|-------------------------|---|
| Output frequency | f ₀ | - | 322.2656 | - | MHz | - |
| Supply voltage | Vcc | -0.5 | - | 4 | V | - |
| Operating temperature | T_use | -5 | - | 85 | °C | - |
| Frequency tolerance | f_tol | -50 | - | 50 | x10 ⁻⁶ | - |
| Current consumption | I _{cc} | - | - | 30 | mA | - |
| Stand-by current | I_std | - | - | - | mA | - |
| Disable current | I_dis | - | - | 15.0 | mA | - |
| Symmetry | SYM | 45 | - | 55 | % | - |
| Output voltage(LVDS) | V _{OD} | 247 | - | 454 | mV | - |
| | dV _{OD} | - | - | 50 | mV | - |
| | V _{OS} | 1.125 | - | 1.375 | V | - |
| | dV _{OS} | - | - | 150 | mV | - |
| Output load condition(LVDS) | L_LVDS | - | 100 | - | Ω | - |
| Input voltage | V _{IH} | 0.7Vcc | - | - | | - |
| | V _{IL} | - | - | 0.3Vcc | | - |
| Rise time | t _r | - | - | 400 | ps | - |
| Fall time | t _f | - | - | 400 | ps | - |
| Start-up time | t_str | - | - | 10 | ms | - |
| Jitter | t _{DJ} | - | - | N/A | ps | Deterministic Jitter |
| | T _{RJ} | - | - | N/A | ps | Random Jitter |
| | t _{RMS} | - | - | N/A | ps | δ(RMS of total distribution) |
| | t _{p-p} | - | - | N/A | ps | Peak to Peak |
| | t _{acc} | - | - | N/A | ps | Accumulated Jitter(δ) n=2 to 50000 cycles |
| Phase jitter | t _{PJ} | - | - | 0.19 | ps | Off set Frequency: 12kHz to 20MHz |
| Phase noise | L(f) | - | - | - | dBc/Hz | Off set 1Hz |
| | | - | -50.7 | - | dBc/Hz | Off set 10Hz |
| | | - | -74.6 | - | dBc/Hz | Off set 100Hz |
| | | - | -101.3 | - | dBc/Hz | Off set 1kHz |
| | | - | -133.9 | - | dBc/Hz | Off set 10kHz |
| | | - | -144.9 | - | dBc/Hz | Off set 100kHz |
| | | - | -147.7 | - | dBc/Hz | Off set 1MHz |
| Frequency aging | f_age | -10 | - | 10 | x10 ⁻⁶ /Year | @+25°C first year |
| | | - | - | - | | - |

3. Test circuit

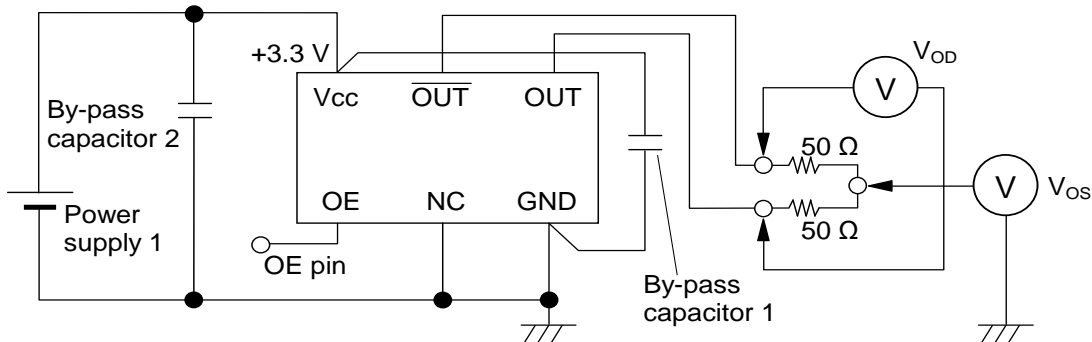
1) To observe waveform and current (case 1)



* The lines from OUT and OUT pin are same length.

* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



* The lines from OUT and OUT pin are same length.

3) Measurement condition

A) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01 μ F to 0.1 μ F) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10 μ F) places closely between power supply terminals on the board.

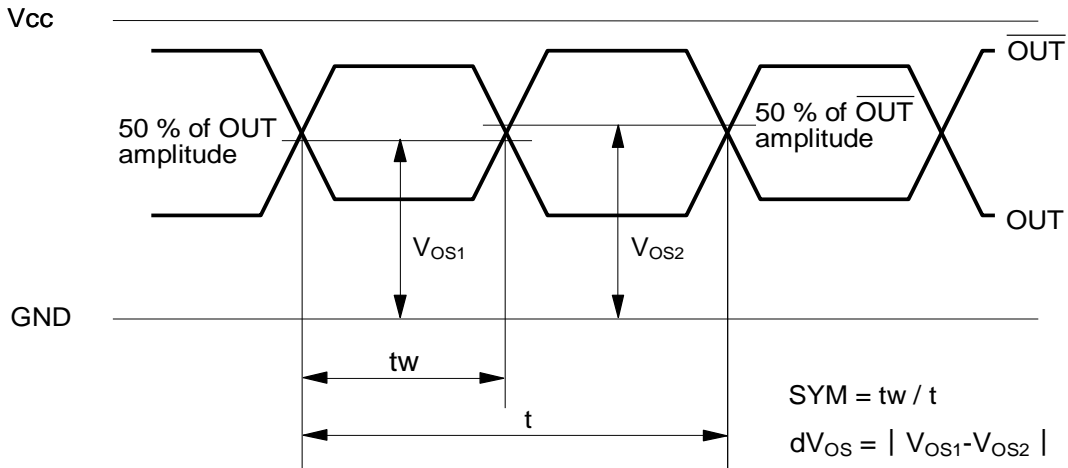
D) Use the current meter whose internal impedance value is small.

E) Power supply

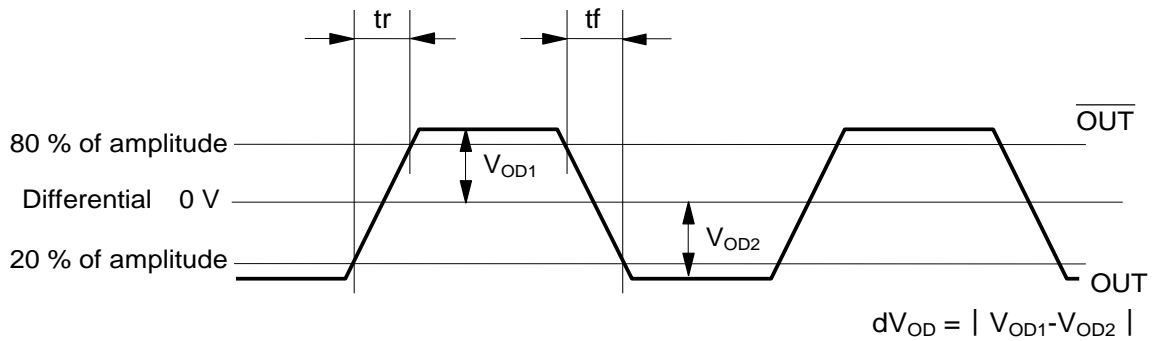
- Start up time (0 Vg90 %Vcc) of power source should be more than 150 μ s and slew rate should be less than 19.8 mV/ μ s.
- Impedance of power supply should be as low as possible.

4.Timing chart

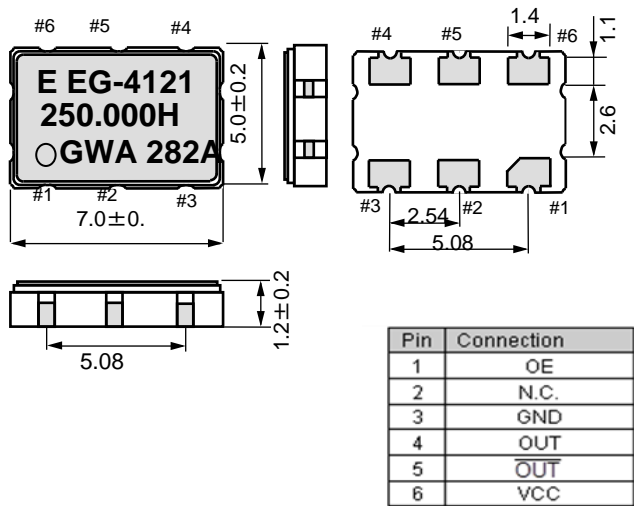
Each output waveform (OUT, and $\overline{\text{OUT}}$)



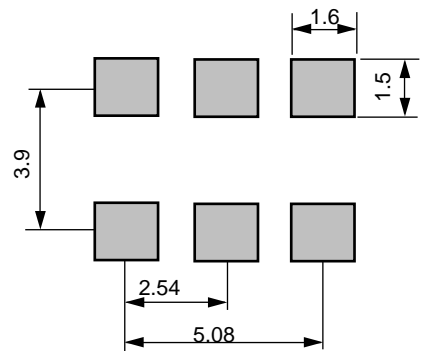
Differential output waveform (OUT – $\overline{\text{OUT}}$)



5.External dimensions (Unit: mm)



6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

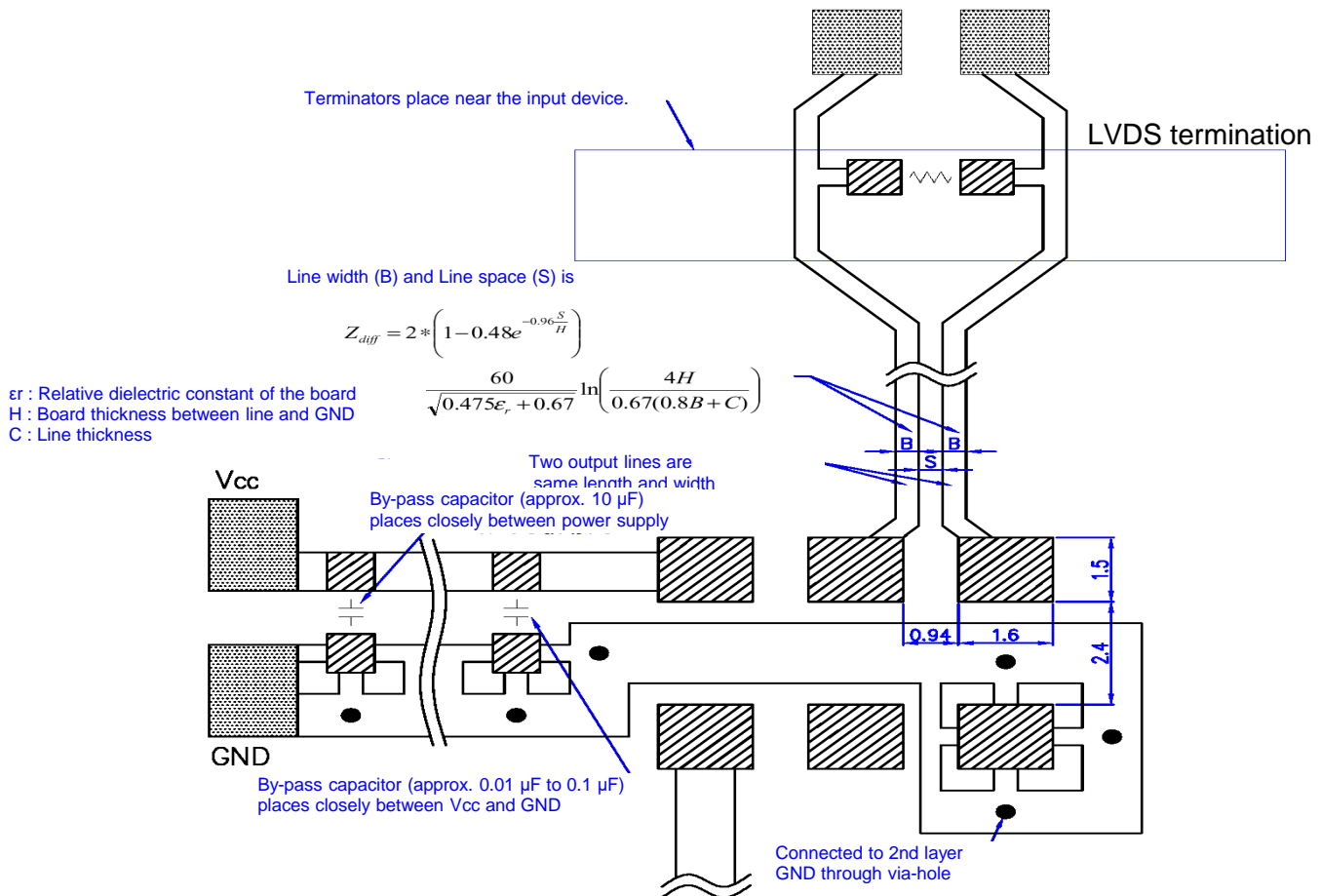
7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)

Temperature [°C]



8.PCB layout (2 layers, 2nd layer is all GND pattern)



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- * By-pass capacitor (approx. 0.01 μ F to 0.1 μ F) places closely between Vcc and GND.
- * By-pass capacitor (approx. 10 μ F) places closely between power supply terminals on the board.
- * Please design the two output lines by characteristic impedance 100 Ω and same length, and try to make the output lines as short as possible.

9.Packing information

[1]Product number last 2 digits code(xx) description

The recommended code is "00"

X1M0003510030xx

| Code | Condition | Code | Condition |
|------|------------------------------|------|----------------|
| 01 | Any Q'ty vinyl bag(Tape cut) | 13 | 500pcs / Reel |
| 11 | Any Q'ty / Reel | 00 | 1000pcs / Reel |
| 12 | 250pcs / Reel | | |

[2] Taping specification

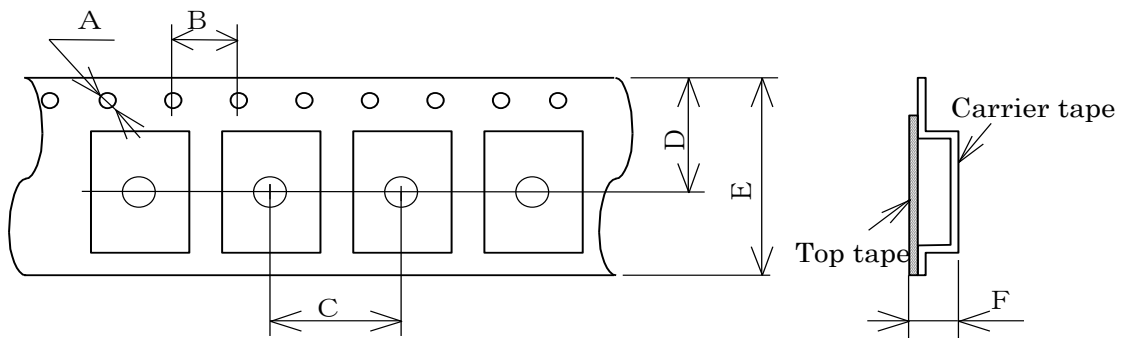
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

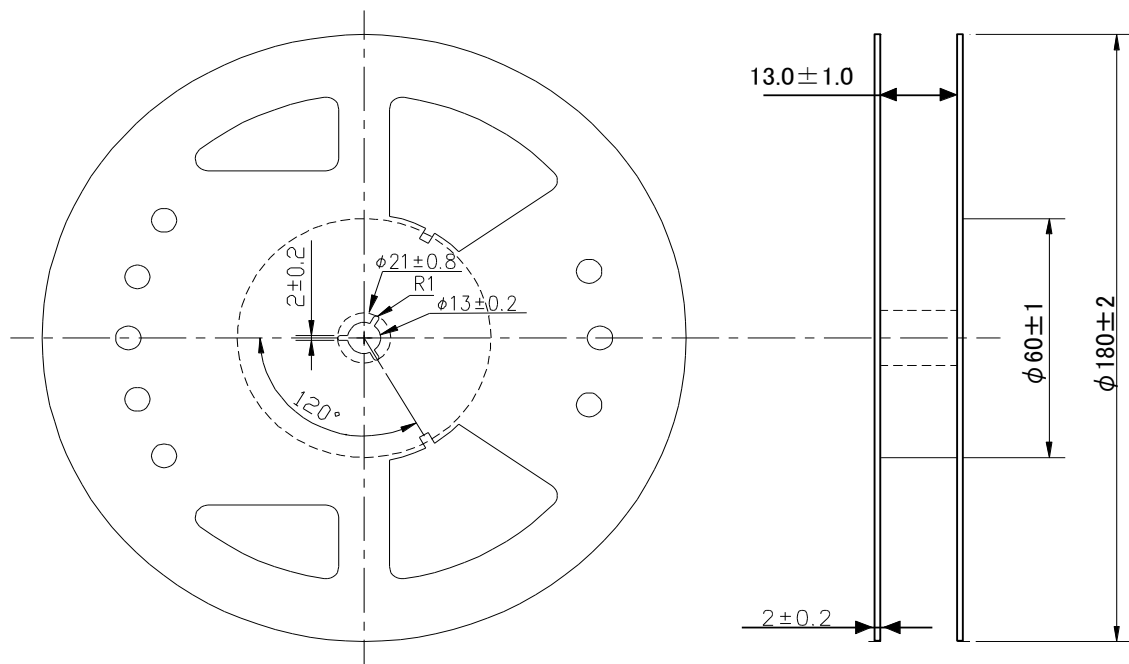


| Symbol | A | B | C | D | E | F |
|--------|------------|---|---|------|----|-----|
| Value | $\phi 1.5$ | 4 | 8 | 9.25 | 16 | 2.3 |

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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