

## Clock OSC

## XG5032HAN

Product name XG5032HAN 100.000000MHz +/-100ppm CLDA

Product Number / Ordering code X1M0004610006xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform HCSL

Pb free / Complies with EU RoHS directive

Reference weight Typ. 70 mg

**1.Absolute maximum ratings**

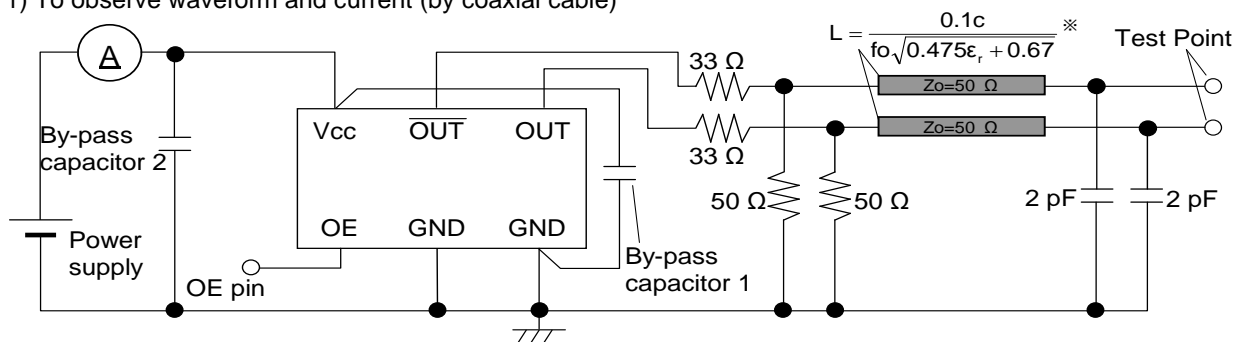
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	V <sub>cc-GND</sub>	-0.5	-	4	V	-
Storage temperature	T <sub>stg</sub>	-55	-	125	°C	Storage as single product
Input voltage	V <sub>in</sub>	-0.5	-	V <sub>cc</sub> +0.5	V	ST or OE Terminal

**2.Specifications(characteristics)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f <sub>0</sub>	-	100.0000	-	MHz	
Supply voltage	V <sub>cc</sub>	2.97	3.3	3.63	V	-
Operating temperature	T <sub>use</sub>	-5	-	85	°C	-
Frequency tolerance	f <sub>tol</sub>	-100	-	100	x10 <sup>-6</sup>	-
Current consumption	I <sub>cc</sub>	-	-	35	mA	OE=V <sub>cc</sub> ,HCSL=50Ω
Stand-by current	I <sub>std</sub>	-	-	-	mA	-
Disable current	I <sub>dis</sub>	-	-	15.0	mA	OE = GND
Symmetry	SYM	45	-	55	%	0
Output voltage(HCSL)	V <sub>OH</sub>	-	0.75	-	V	-
	V <sub>OL</sub>	-	0	-	V	-
Crossing voltage	V <sub>CR</sub>	0.25	-	0.55	V	-
Output load condition(LVDS)	L <sub>LVDS</sub>	-	50	-	Ω	Terminal to GND
	R <sub>S</sub>	-	33	-	Ω	-
	C <sub>L</sub>	-	2	-	pF	-
Input voltage	V <sub>IH</sub>	0.7V <sub>cc</sub>	-	-		-
	V <sub>IL</sub>	-	-	0.3V <sub>cc</sub>		-
Rise time	t <sub>r</sub>	1	-	4	ps	[V/n]
Fall time	t <sub>f</sub>	1	-	4	ps	[V/n]
Start-up time	t <sub>str</sub>	-	-	10	ms	-
Jitter	t <sub>DJ</sub>	-	-	N/A	ps	Deterministic Jitter
	T <sub>RJ</sub>	-	-	N/A	ps	Random Jitter
	t <sub>RMS</sub>	-	-	N/A	ps	δ(RMS of total distribution)
	t <sub>p-p</sub>	-	-	N/A	ps	Peak to Peak
	t <sub>acc</sub>	-	-	N/A	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t <sub>PJ</sub>	-	-	0.3	ps	Off set Frequency: 12kHz to 20MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Off set 1Hz
		-	-61.3	-	dBc/Hz	Off set 10Hz
		-	-91.2	-	dBc/Hz	Off set 100Hz
		-	-119.5	-	dBc/Hz	Off set 1kHz
		-	-144.6	-	dBc/Hz	Off set 10kHz
		-	-153.6	-	dBc/Hz	Off set 100kHz
Frequency aging	f <sub>age</sub>	-	-	-	x10 <sup>-6</sup> /Year	Included in Frequency tolerance 10 years
		-	-	-		-

### 3. Test circuit

- 1) To observe waveform and current (by coaxial cable)



- \* Each output line is same length.
- \* To measure the disable current, OE pin is connected to GND.
- \*  $L=176\text{mm}$  (about 7 inch) when  $f_0=100\text{ MHz}$ ,  $\epsilon_r=4.7$  (FR-4)

- 2) Measurement condition

- (1) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

- (2) By-pass capacitor 1 (approx.  $0.01\text{ }\mu\text{F}$  to  $0.1\text{ }\mu\text{F}$ ) places closely between Vcc and GND.

- (3) By-pass capacitor 2 (approx.  $10\text{ }\mu\text{F}$ ) places closely between power supply terminals on the board.

- (4) Use the current meter whose internal impedance value is small.

- (5) Output line length L is estimated as follows

$$L = \frac{0.1c}{f_0 \sqrt{0.475\epsilon_r + 0.67}}$$

$\epsilon_r$  : Relative dielectric constant of the board

$f_0$  : Output frequency

$c$  : Velocity of light in a vacuum

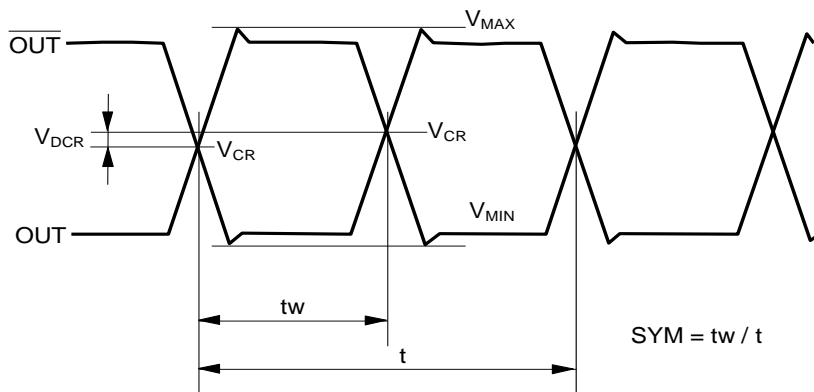
- (6) Power supply

- Start up time ( $0\text{ V} \rightarrow 90\%V_{cc}$ ) of power source should be more than  $150\text{ }\mu\text{s}$  and slew rate should be less than  $19.8\text{ mV}/\mu\text{s}$ .
- Impedance of power supply should be as low as possible.

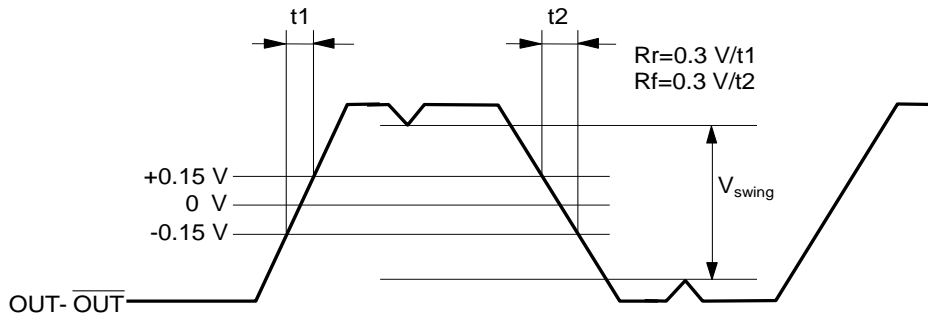
### 4. Timing chart

- 1) Output waveform and level

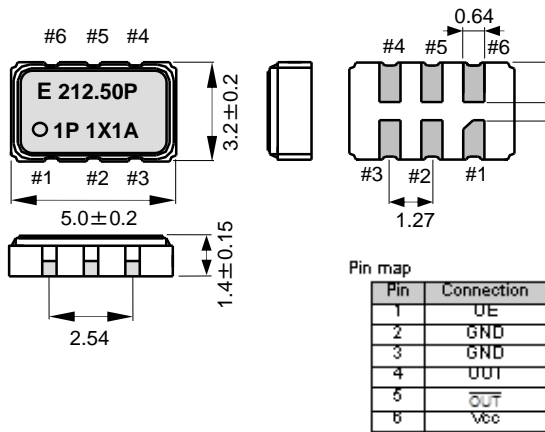
- OUT and OUT-bar



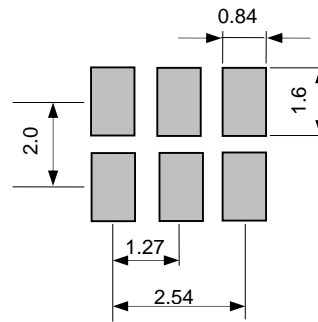
• OUT-OUT



### 5.External dimensions (Unit: mm)



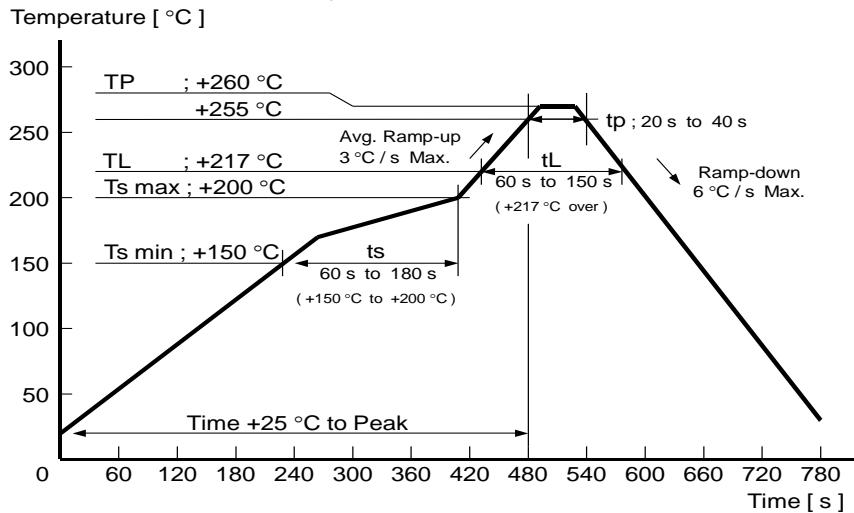
### 6.Footprint(Recommended) (Unit: mm)



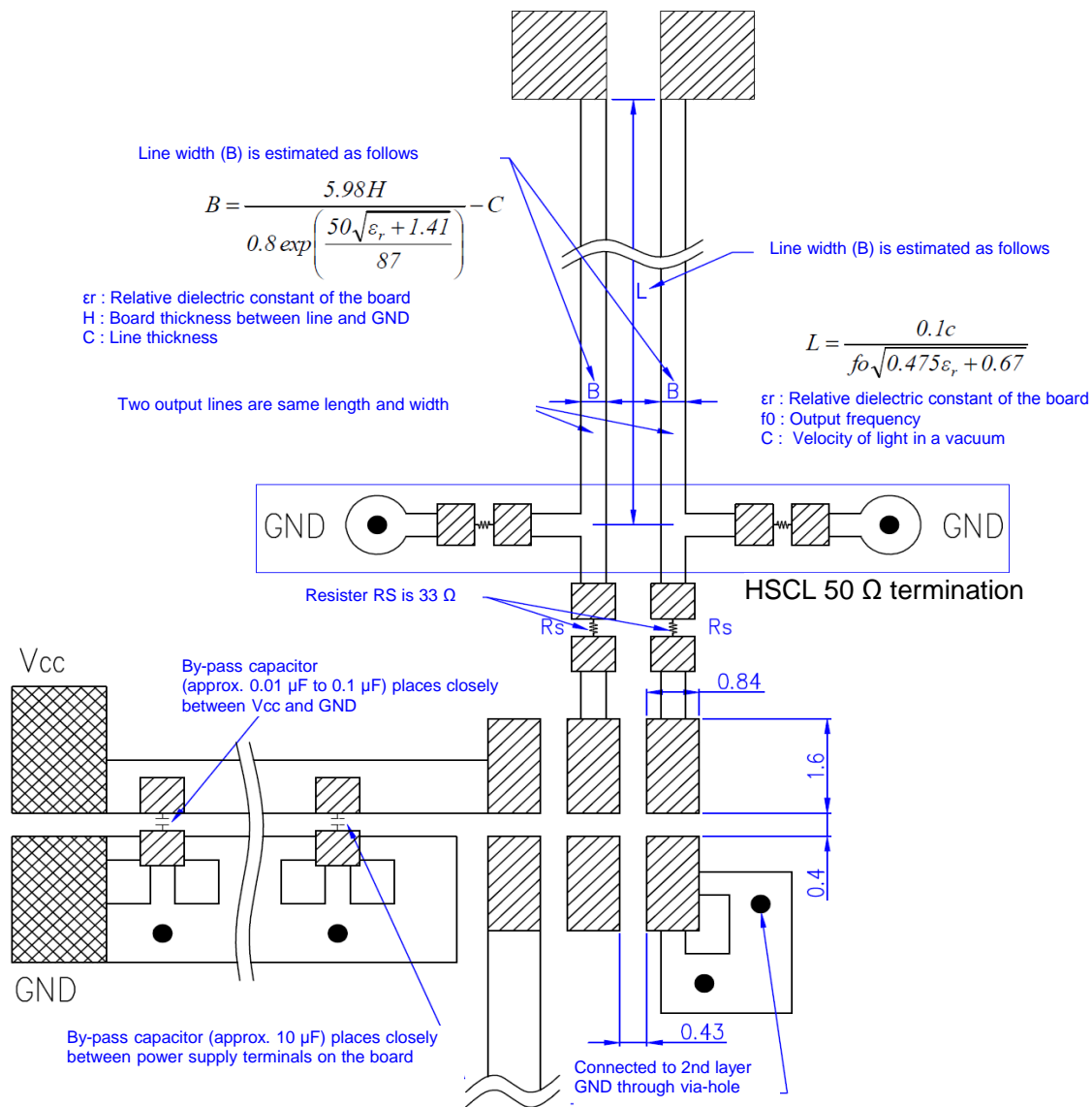
To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

### 7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



## 8.PCB layout (2 layers, 2nd layer is all GND pattern)



- \* By-pass capacitor (approx. 0.01  $\mu F$  to 0.1  $\mu F$ ) places closely between  $V_{CC}$  and GND.
  - \* By-pass capacitor (approx. 10  $\mu F$ ) places closely between power supply terminals on the board.
  - \* Please design the two output lines by characteristic impedance 50  $\Omega$  and same length,
  - \* Reflection wave occurs in two output lines after 50  $\Omega$  terminal resistances.
- In the case except output line length  $L$  shown in the upper figure, reflection wave may influence the rise and fall waveform and electric characteristic may not satisfy this specifications.

## 9.Packing information

[ 1 ] Product number last 2 digits code(xx) description

The recommended code is "00"

X1M0004610006xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

## [ 2 ] Taping specification

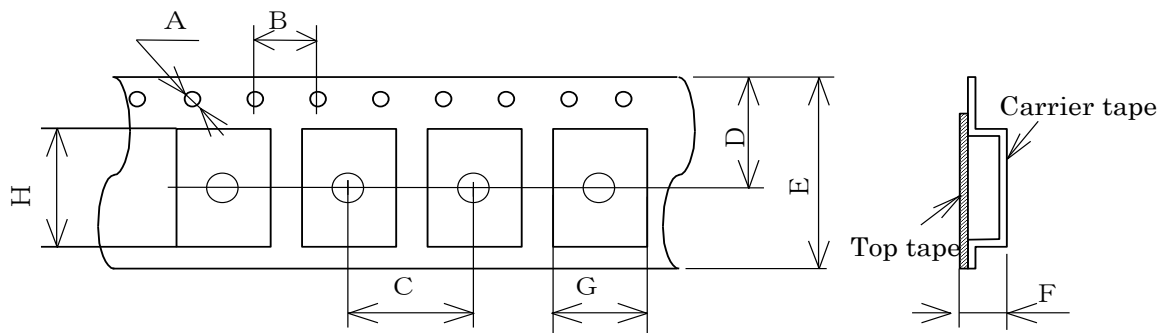
Subject to EIA-481 &amp; IEC-60286

## (1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

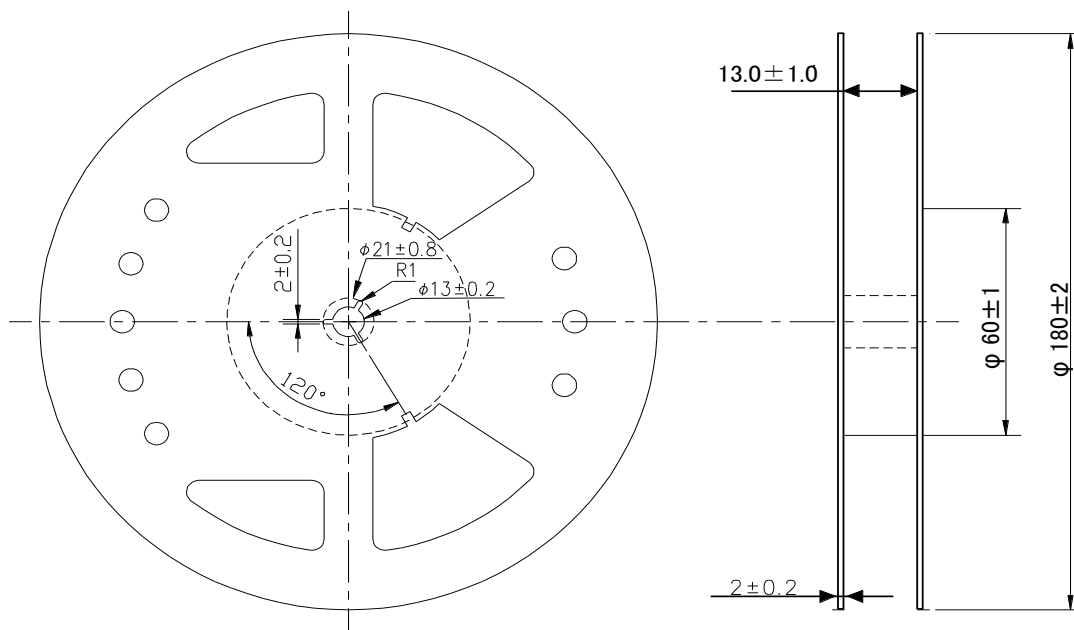


Symbol	A	B	C	D	E	F	G	H
Value	$\phi 1.5$ $+0.1/-0$	$4.0 \pm 0.1$	$8.0 \pm 0.1$	$7.25 \pm 0.2$	$12.0 \pm 0.2$	$1.40 \pm 0.1$	$3.5 \pm 0.1$	$5.4 \pm 0.1$

## (2) Reel dimensions

Center material : PS

Material of the Reel : PS



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